What is claimed is:

1. A clock monitoring apparatus comprising:

a main clock monitoring portion including a first counter for counting a main clock, issuing a normal operation confirming flag indicating that a normal operation is being carried out when the first counter is overflowed or reaches a previously determined set value, monitoring the normal operation confirming flag by a sub clock, issuing a first main clock stop flag having an output in correspondence with H (high level) / L (low level) of the normal operation confirming flag and a main clock initializing signal for initializing the main clock when the main clock is determined to stop and resetting the first main clock stop flag when the main clock is recovered by receiving the main clock initializing signal; and

a sub clock switching control portion including a second counter for counting a signal output produced by calculating a logical sum of the sub clock and the first main clock stop flag at fall of the sub clock at a time point of generating the first main clock stop flag, switching to a sub clock operation by issuing a sub clock switching signal when the second counter output is overflowed or reaches a previously determined set value and resetting the second counter output when the main clock is recovered and a second main clock stop flag produced by inverting the first main clock stop flag and delaying the sub clock by a predetermined period by a main clock monitoring portion, is reset.

2. The clock monitoring apparatus according to Claim 1, wherein the second main clock stop flag generating portion outputs the main clock initializing signal by calculating a logical sum of the first main clock stop flag and the second main clock stop flag.

3. The clock monitoring apparatus according to Claim 2, further comprising:

a first logical product circuit for calculating a logical product of a main clock temporarily stopping signal for temporarily stopping the main clock and an output signal from the first logical sum circuit; and

a second logical product circuit for calculating a logical product of the main clock temporarily stop signal and an output signal from the second counter.

4. The clock monitoring apparatus according to Claim 1, wherein the main clock monitoring portion comprising:

a main clock monitoring circuit for counting the main clock by the first counter, issuing the normal operation confirming flag when the first counter is equal to the predetermined set value or overflowed and monitoring the normal operation confirming flag at fall of the sub clock;

a first main clock stop flag generating portion for issuing the first main clock stop flag constituting "H" when the normal operation confirming flag is "H" and constituting

"L" when the normal operation confirming flag is "L" at fall of the sub clock; and

a second main clock stop flag generating portion for issuing the second main clock stop flag and the main clock initializing signal when the main clock is stopped.

5. The clock monitoring apparatus according to Claim 1, wherein when the main clock is recovered by receiving the main clock initializing signal, the main clock monitoring portion resets the second main clock stop flag.

6. The clock monitoring apparatus according to Claim 1, wherein the sub clock switching control portion includes a second logical sum circuit for calculating a logical sum of the first main clock stop flag and the sub clock, making the second counter count the logical sum signal at a time point of generating the main clock stop flag, switching to the sub clock operation by issuing the sub clock switching signal when the second counter is overflowed or reaches the set value and returning to a standby state by resetting the second counter when the main clock is recovered and the main clock stop flag is reset.

7. The clock monitoring apparatus according to Claim 6, wherein in a case in which the main clock stays to be stopped even when the main clock is stopped and the main microcomputer is initialized, the second counter is overflowed and a sub

clock switching signal is issued by the sub clock switching control portion.

8. The clock monitoring apparatus according to Claim 1, further comprising:

a sub clock self monitoring portion capable of issuing an all clock stop flag indicating that all the clocks are stopped when the sub clock is stopped, initializing automatically the main clock when the main clock is stopped and carrying out a continuing operation under a state before abnormality when the main clock is recovered thereby.

9. The clock monitoring apparatus according to Claim 8:

wherein the sub clock self monitoring portion comprising:

a first delaying adding circuit for issuing a first delay signal for delaying the sub clock by a predetermined period and a second delay adding circuit for issuing a second delay signal for delaying the first delay signal by the predetermined period;

an exclusive-OR circuit for calculating an exclusive-OR of the sub clock, the first delay signal and the second delay signal; and

a third logical product circuit for calculating a logical product of the second main clock stop flag and an inverted signal of a signal produced by calculating the exclusive-OR;

wherein an all clock stop flag is outputted from the

third logical product circuit.

10. The clock monitoring apparatus according to Claim 9, further comprising:

a first logical product circuit for calculating a logical product of a main clock temporarily stopping signal for temporarily stopping the main clock and an output signal from the first logical sum circuit;

a second logical product circuit for calculating a logical product of the main clock temporarily stopping signal and an output signal from the second counter; and

a third logical product circuit for calculating a logical product of the main clock temporarily stopping signal and an output signal from the third logical sum circuit.